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S39	13	S38 and (timing with element with (set or collection))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 14:40
S38	111	S30 and (delay with element) and (timing with element) and circuit	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 13:39
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S34	2	S33 and (delay or delays)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 13:36
S33	2	S30 and S32	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 13:35
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S30	566	(static adj timing adj analy$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 13:35

S31	1	S30 and ((timing adj (element or set or model or characteristic)) same (replac$4 or substitut$4 or swap$4 or switch$4) same (timing adj (block or circuit$3)))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 13:08
S28	41	S21 and (timing adj (element or set or model or characteristic)) and (replac$4 or substitut$4 or swap$4 or switch$4) and (timing adj (block or circuit$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 12:36
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S27	1	S21 and S25	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 10:48
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S24	9454	(timing with (element or set or model or characteristic)) same (replac$4 or substitut$4 or swap$4 or switch$4) same (timing with (block or circuit$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 10:35
S23	680	(timing with (element or set or model or characteristic)) same (replac$4 or substitut$4 or swap$4 or switch$4) same (timing with (block or citcuit$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 10:35
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S18	5839	(timing adj set)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 09:41

S17	0	S16 and (timing adj set)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 09:41
S16	34	S15 and (timing or time)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 09:40
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S2	30	S1 and (timing or time)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/28 09:40
S14	23	S13 and ((element or circuit or block or component) with set)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/15 09:42
S13	57	(worst same case same timing same path) and (best same case same timing same path)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/15 09:42
S12	22	S9 and ((element or circuit or block) with set)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/15 09:42
S11	32	S9 and element	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:31
S10	35	S9 and circuit same (simulat$5 or emulat$5 or model$5)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:30
S9	57	(worst same case same timing same path) and (best same case same timing same path)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:30
S8	5	("6021261" "5651012" "5790830" "6083273" "6158022").pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:28

S7	1	S6 and (static with timing)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:18
S6	39	timing adj determin$5 adj block	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:15
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S3	21	S2 and ((timing or time) with (element or circuit or block))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 21:03
S1	34	(AMATANGELO-MATTHEW-J KHWAJA-ZAKARIA LEVY-HOWARD LEVY-HOWARD-L LEVY-HOWARD-LAWRENCE LEVY-HOWARD-M LEVY-HOWARD-S PAREDES-JOSE PAREDES-JOSE-A PAREDES-JOSE-ANGEL PATEL-BINTA-M PATEL-BINTA-MINESH).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2004/11/12 20:51

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Fassnacht, U.; Schietke, J.;
Design, Automation and Test in Europe, 1998., Proceedings
23-26 Feb. 1998 Page(s):325 - 331
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February 2005 (Vol. 38, No. 2)

pp. 53-61 • Transistor-Level Optimization of Digital Designs with Flex Cells

Rob Roy, Debashis Bhattacharya, Vamsi Boppana,
Zenasis Technologies

Over the years, it has become commonplace to perform various forms of manual intervention ondesigns generated using automated flows. The quest to overcome the limitations of standard-cell-based design methods leads naturally to the creation of new design- and context-specific cells—designated flex cells—during the process of optimizing a given digital design. Flex cell—based design optimization automates the creation of tactical cells.

The flex-cell approach, either alone or in combination with standard cells, provides an optimally tuned set of building blocks for the target IC design, which measures optimality against accepted and quantifiably definable metrics such as clock speed, die size, and power consumption. By allowing manipulation of the transistor-level structures, flex cells open up a new dimension in theoptimization of automatically created designs.

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1 Session 8D: Timing and noise analysis: A symbolic simulation-based methodology for generating black-box timing models of custom macrocells
Clayton B. McDonald, Randal E. Bryant
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(110.81 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a methodology for generating black-box timing models for full-custom transistor-level CMOS circuits. Our approach utilizes transistor-level ternary symbolic timing simulation to explore the input arrival time space and determine the input arrival time windows that result in proper operation. This approach integrates symbolic timing simulation into existing static timing analysis flows and allows automated modelling of the timing behavior of aggressive full-custom circuit design styles ...

2 Static timing analysis for self resetting circuits
Vinod Narayanan, Barbara A. Chappell, Bruce M. Fleischer
January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(413.77 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Static timing analysis techniques are widely used to verify the timing behavior of large digital designs implemented predominantly in conventional static CMOS. These techniques, however, are not sufficient to completely verify the dynamic circuit families now finding favor in high-performance designs. In this paper, we describe an approach that extends static timing analysis to a high-performance dynamic CMOS logic family called self-resetting CMOS. Due to the circuit structure employed in SRCMO ...

3 Timing abstraction: Automated timing model generation
Ajay J. Daga, Loa Mize, Subramanyam Sripada, Chris Wolff, Qiuyang Wu
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(260.13 KB) Additional Information: full citation, abstract, references, index terms

The automated generation of timing models from gate-level netlists facilitates IP reuse and dramatically improves chip-level STA runtime in a hierarchical design flow. In this paper we discuss two different approaches to model generation, the design flows they lend themselves to and results from the application of these model generation solutions to large

customer designs.

Keywords: EDA, model generation, static timing analysis

4 Timing abstraction: Timing model extraction of hierarchical blocks by graph reduction
Cho W. Moon, Harish Kriplani, Krishna P. Belkhale
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(199.64 KB) Additional Information: full citation, abstract, references, index terms

Timing model extractor builds a timing model of a digital circuit for use with a static timing analyzer. This paper proposes a novel method of generating a gray box timing model from gate-level netlist by reducing a timing graph. Previous methods of generating timing models sacrificed accuracy and/or did not scale well with design size. The proposed method is simple, yet it provides model accuracy including arbitrary levels of latch time borrowing and capability to support timing constraints tha ...

5 Timing analysis and optimization of a high-performance CMOS processor chipset
U. Fassnacht, J. Schietke
February 1998 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(56.10 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We describe the timing analysis and optimization methodology used for the chipset inside the IBM S/390 Parallel Enterprise Server - Generation 3. After an introduction to the concepts of static timing analysis, we describe the timing-modeling for the gates and interconnects, explain the optimization schemes and present obtained results.

Keywords: Timing, timing optimization, static timing analysis

6 Design for manufacturing: Toward a systematic-variation aware timing methodology
Puneet Gupta, Fook-Luen Heng
June 2004 **Proceedings of the 41st annual conference on Design automation**
Full text available: pdf(229.54 KB) Additional Information: full citation, abstract, references, index terms

Variability of circuit performance is becoming a very important issue for ultra-deep sub-micron technology. Gate length variation has the most direct impact on circuit performance. Since many factors contribute to the variability of gate length, recent studies have modeled the variability using Gaussian distributions. In reality, the through-pitch and through-focus variations of gate length are systematic. In this paper, we propose a timing methodology which takes these systematic variations int ...

Keywords: ACLV, OPC, layout, lithography, manufacturability

7 Highlights of ISSCC: high-speed heterogenous design techniques: A reconfigurable signal processing IC with embedded FPGA and multi-port flash memory
M. Borgatti, L. Calì, G. De Sandre, B. Forêt, D. Iezzi, F. Lertora, G. Muzzi, M. Pasotti, M. Poles, P. L. Rolandi
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(402.77 KB) Additional Information: full citation, abstract, references, citings, index terms

A 1GOPS dynamically reconfigurable processing unit with embedded Flash memory and SRAM-based FPGA targets image-voice processing and recognition applications. Code, data

and FPGA bitstreams are stored in the embedded Flash memory and are independently accessible through 3 content-specific, 64-bit I/O ports with a peak read rate of 1.2GB/s. The system is implemented in a 0.18um, 2PL-6ML CMOS Flash technology, chip area is 70mm2.

Keywords: application-specific integrated circuits (ASICs), digital signal processors, field-programmable gate arrays (FPGAs), integrated circuit design, multimedia computing, reconfigurable architectures

8 Test point insertion: scan paths through combinational logic

Chih-chang Lin, Malgorzata Marek-Sadowska, Kwang-Ting Cheng, Mike Tien-Chien Lee
June 1996 **Proceedings of the 33rd annual conference on Design automation**

Full text available: pdf(323.60 KB) Additional Information: full citation, references, citings, index terms

9 ASIC design in nanometer era - dead or alive?: Designing mega-ASICs in nanogate technologies

David E. Lackey, Paul S. Zuchowski, Juergen Koehl
June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(264.47 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses challenges the designer faces in integrating entire system product designs, containing tens or even hundreds of millions of logic gates, into single chip solutions now within reach using circuit densities possible in the latest silicon technologies. Managing designs of this size presents a new dimension of issues, and managing the physical and electrical effects of these high density device geometries presents another; solutions in both these areas are presented. Lastly, thi ...

Keywords: design productivity, methodology, power management, signal integrity, system-on-chip, time to market

10 Highlights of ISSCC and the design of state-of-the-art microprocessors: A 1.5GHz third generation itanium® 2 processor

Jason Stinson, Stefan Rusu
June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(403.60 KB) Additional Information: full citation, abstract, references, index terms

This 130nm Itanium® 2 processor implements the Explicitly Parallel Instruction Computing (EPIC) architecture and features an on-die 6MB, 24-way set associative L3 cache. The 374mm2 die contains 410M transistors and is implemented in a dual-Vt process with 6 layers copper interconnect and FSG dielectric. The processor runs at 1.5GHz at 1.3V and dissipates a maximum of 130W. This paper reviews circuit design and package details, power delivery, RAS, DFT and DFM features, as well as an overvie ...

Keywords: design methodology, on-die cache, processor, reliability, test

11 Timing abstraction: Efficient stimulus independent timing abstraction model based on a new concept of circuit block transparency

Martin Foltin, Brian Foutz, Sean Tyler
June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(68.50 KB) Additional Information: full citation, abstract, references, index terms

We have developed a new timing abstraction model for digital circuit blocks that is stimulus

independent, port based, supports designs with level triggered latches, and can be input into commercial STA (Static Timing Analysis) tools. The model is based on an extension of the concept of latch transparency to circuit block transparency introduced in this paper. It was implemented, tested and is being used in conjunction with transistor level STA for microprocessor designs with tens of millions of ...

Keywords: VLSI design, circuit optimization, timing analysis, timing model

12 Advanced test solutions: On path-based learning and its applications in delay test and diagnosis

Li-C. Wang, T. M. Mak, Kwang-Ting Cheng, Magdy S. Abadir

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(447.54 KB) Additional Information: full citation, abstract, references, index terms

This paper describes the implementation of a novel path-based learning methodology that can be applied for two purposes: (1) In a pre-silicon simulation environment, path-based learning can be used to produce a fast and approximate simulator for statistical timing simulation. (2) In post-silicon phase, path-based learning can be used as a vehicle to derive critical paths based on the pass/fail behavior observed from the test chips. Our path-based learning methodology consists of four major compo ...

Keywords: delay test, machine learning, statistical timing simulation

13 Novel design methodologies and signal integrity: Static noise analysis with noise windows

Ken Tseng, Vinod Kariat

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(122.54 KB) Additional Information: full citation, abstract, references, citings, index terms

As processing technology scales down to the nanometer regime, capacitive crosstalk is having an increasingly adverse effect on circuit functionality, leading to increasing number of chip failures. In this paper, we propose mapping the static crosstalk functional noise problem into the well understood static timing problem. The key differences between static noise and static timing analyses, namely the injection of noise, accurate noise window propagation and register sensitive window computation ...

Keywords: crosstalk, noise, signal integrity

14 Design for manufacturability and global routing: A cost-driven lithographic correction methodology based on off-the-shelf sizing tools

P. Gupta, A. B. Kahng, D. Sylvester, J. Yang

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(149.73 KB) Additional Information: full citation, abstract, references, citings, index terms

As minimum feature sizes continue to shrink, patterned features have become significantly smaller than the wavelength of light used in optical lithography. As a result, the requirement for dimensional variation control, especially in critical dimension (CD) 3σ, has become more stringent. To meet these requirements, resolution enhancement techniques (RET) such as optical proximity correction (OPC) and phase shift mask (PSM) technology are applied. These approaches result in a substantial inc ...

Keywords: OPC, RET, VLSI manufacturability, lithography, yield

15 Issues in crosstalk: Efficient switching window computation for cross-talk noise
Bhavana Thudi, David Blaauw
December 2002 **Proceedings of the 8th ACM/IEEE international workshop on Timing issues in the specification and synthesis of digital systems**
Full text available: pdf(182.45 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present an efficient method for computing switching windows in the presence of delay noise. In static timing analysis, delay noise has traditionally been modeled using a simple switch-factor based noise model and the computation of switching windows is performed using an iterative algorithm where timing window propagation and switch factor updates are computed repeatedly until convergence. It was shown that the worst-case number of iterations required for convergence is O(*n*< ...

16 New directions in timing analysis: From blind certainty to informed uncertainty
Kurt Keutzer, Michael Orshansky
December 2002 **Proceedings of the 8th ACM/IEEE international workshop on Timing issues in the specification and synthesis of digital systems**
Full text available: pdf(243.42 KB) Additional Information: full citation, abstract, references, citings, index terms

The accuracy, computational efficiency, and reliability of static timing analysis have made it the workhorse for verifying the timing of synchronous digital integrated circuits for more than a decade. In this paper we charge that the traditional deterministic approach to analyzing the timing of circuits is significantly undermining its accuracy and may even challenge its reliability. We argue that computation of the static timing of a circuit requires a dramatic rethinking in order to continue s ...

17 Delay and noise modeling in the nanometer regime: Non-iterative switching window computation for delay-noise
Bhavana Thudi, David Blaauw
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(138.38 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we present an efficient method for computing switching windows in the presence of delay noise. In static timing analysis, delay noise has traditionally been modeled using a simple switch-factor based noise model and the computation of switching windows is performed using an iterative algorithm, resulting in an overall run time of O(n2), where n is the number of gates in the circuit. It has also been shown that the iterations converge to different solutions, depending on the initia ...

Keywords: cross-talk noise, superposition, switching window

18 Delay estimation VLSI circuits from a high-level view
Mahadevamurty Nemani, Farid N. Najm
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**
Full text available: pdf(180.14 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

Estimation of the delay of a Boolean function from its functional description is an important step towards design exploration at the register transfer level (RTL). This paper addresses

the problem of estimating the delay of certain optimal multi-level implementations of combinational circuits, given only their functional description. The proposed delay model uses a new complexity measure called the delay measure to estimate the delay. It has an advantage th ...

19 Functional timing analysis for IP characterization

Hakan Yalcin, Mohammad Mortazavi, Robert Palermo, Cyrus Bamji, Karem Sakallah

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(647.16 KB) Additional Information: full citation, references, citings, index terms

Keywords: IP characterization, false path, functional (mode) dependency, timing analysis

20 The usage of stochastic processes in embedded system specifications

Axel Jantsch, Ingo Sander, Wenbiao Wu

April 2001 **Proceedings of the ninth international symposium on Hardware/software codesign**

Full text available: pdf(571.75 KB) Additional Information: full citation, abstract, references, citings, index terms

We review the use of nondeterminism and identify two different purposes. The *descriptive purpose* handles uncertainties in the behaviour of existing entities. The *constraining purpose* is used in specifications to constrain implementations. For the specification of embedded systems we suggest a *stochastic processor* instead of nondeterminism. It serves mostly the descriptive purpose but can also be used to constrain the system. We carefully distinguish different interpretati ...

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21 Crosstalk Noise: On convergence of switching windows computation in presence of crosstalk noise

Pinhong Chen, Yuji Kukimoto, Chin-Chi Teng, Kurt Keutzer

April 2002 **Proceedings of the 2002 international symposium on Physical design**

Full text available: pdf(114.76 KB) Additional Information: full citation, abstract, references, citings, index terms

Detecting overlapping of switching windows between coupling nets is a major static technique to accurately locate crosstalk noise. However, due to the mutual dependency between switching windows, the computation requires iterations to converge. In this paper, we discuss the issues and provide answers to the important questions involved in convergence and numerical properties, including the effect of coupling models, multiple convergence points, convergence rate, computational complexity, non-mon ...

22 Functional correlation analysis in crosstalk induced critical paths identification

Tong Xiao, Malgorzata Marek-Sadowska

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(60.06 KB) Additional Information: full citation, abstract, references, citings, index terms

In deep submicron digital circuits capacitive couplings make delay of a switching signal highly dependent on its neighbors switching times and switching directions. A long path may have a large num-ber of coupling neighbors with difficult to determine interdepen-dencies. Ignoring the mutual relationship among the signals may result in a very pessimistic estimation of circuit delay. In this paper, we apply efficient functional correlation analysis techniques to identify critical paths caused ...

23 False path exclusion in delay analysis of RTL-based datapath-controller designs

C. Papachristou, M. Nourani

September 1996 **Proceedings of the conference on European design automation**

Full text available: pdf(334.54 KB) Additional Information: full citation, references, index terms

24 Timing analysis with crosstalk as fixpoints on complete lattice

Hai Zhou, Narendra Shenoy, William Nicholls

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(230.52 KB) Additional Information: full citation, abstract, references, citings, index terms

Increasing delay variation due to crosstalk has a dramatic impact on deep sub-micron technologies. It is now necessary to include crosstalk in timing analysis. But timing analysis with crosstalk is a chicken-and-egg problem since crosstalk effect in turn depends on timing behavior of a circuit. In this paper, we establish a theoretical foundation for timing analysis with crosstalk. We show that solutions to the problem are fixpoints on a complete lattice. Base on that, we prove in general t ...

25 A new gate delay model for simultaneous switching and its applications

Liang-Chi Chen, Sandeep K. Gupta, Melvin A. Breuer

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(163.26 KB) Additional Information: full citation, abstract, references, citings, index terms

26 Timing verification of sequential domino circuits

David Van Campenhout, Trevor Mudge, Karem A. Sakallah

January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(88.95 KB) Additional Information: full citation, abstract, references, index terms

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Two methods are presented for static timing verification of sequential circuits implemented as a mix of static and domino logic. Constraints for proper operation of domino gates are derived. An important observation is that input signals to domino gates may start changing near the end of the evaluate phase. The first method models domino gates explicitly, similar to latches. The second method treats domino gates only during pre- and post-processing steps. This method is shown to be more conserva ...

Keywords: domino gates, input signals, logic testing, sequential domino circuits, static timing verification

27 Session 3A: Sequential synthesis: Placement driven retiming with a coupled edge timing model

Ingmar Neumann, Wolfgang Kunz

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(136.00 KB) Additional Information: full citation, abstract, references, citings, index terms

Retiming is a widely investigated technique for performance optimization. It performs powerful modifications on a circuit netlist. However, often it is not clear, whether the predicted performance improvement will still be valid after placement has been performed. This paper presents a new retiming algorithm using a highly accurate timing model taking into account the effect of retiming on capacitive loads of single wires as well as fanout systems. We propose the integration of retiming into a t ...

28 Clock Scheduling and Clocktree Construction for High Performance ASICS

Stephan Held, Bernhard Korte, Jens Maßberg, Matthias Ringe, Jens Vygen

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(384.60 KB) Additional Information: full citation, abstract, index terms

In this paper we present a new method for clock schedulingand clocktree construction that improves the performance ofhigh-end ASICs significantly.First, we compute a clock schedule that yields the optimumcycle time and the best possible clock distribution with respectto early and late mode; in particular the number of criticaltests is minimized. Second, individual arrival time intervalsare computed for all endpoints of the clocktree. Finally, weconstruct a clocktree that realizes arrival times w ...

29 (Special session) embedded tutorial: DFM in Nm-process generation: Toward stochastic design for digital circuits: statistical static timing analysis

Shuji Tsukiyama

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair 2004**

Full text available: pdf(197.96 KB) Additional Information: full citation, abstract, references

Due to the process variations and the variations of environmental factors such as supply voltage and temperature, the circuit parameters and hence the circuit performance such as delay fluctuate, and their variability and uncertainty are increasing in the deep sub-micron technology. Therefore, producing high performance digital circuits in high yield becomes difficult more and more. Various efforts have been done in order to analyze and reduce such fluctuations. Among them, statistical static ti ...

30 Managing power and performance for System-on-Chip designs using Voltage Islands

David E. Lackey, Paul S. Zuchowski, Thomas R. Bednar, Douglas W. Stout, Scott W. Gould, John M. Cohn

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(96.51 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper discusses Voltage Islands, a system architecture and chip implementation methodology, that can be used to dramatically reduce active and static power consumption for System-on-Chip (SoC) designs. As technology scales for increased circuit density and performance, the need to reduce power consumption increases in significance as designers strive to utilize the advancing silicon capabilities. The consumer product market further drives the need to minimize chip power consumption.Effectiv ...

31 Statistical timing analysis: First-order incremental block-based statistical timing analysis

C. Visweswariah, K. Ravindran, K. Kalafala, S. G. Walker, S. Narayan

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(215.65 KB) Additional Information: full citation, abstract, references, index terms

Variability in digital integrated circuits makes timing verification an extremely challenging task. In this paper, a canonical first order delay model is proposed that takes into account both correlated and independent randomness. A novel linear-time block-based statistical timing algorithm is employed to propagate timing quantities like arrival times and required arrival times through the timing graph in this canonical form. At the end of the statistical timing, the sensitivities of all timing ...

Keywords: incremental, statistical timing, variability

32 Issues in timing analysis: Worst-case circuit delay taking into account power supply variations

Dionysios Kouroussis, Rubil Ahmadi, Farid N. Najm

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(197.13 KB) Additional Information: full citation, abstract, references, index terms

Current Static Timing Analysis (STA) techniques allow one to verify the timing of a circuit at different process corners which only consider cases where all the supplies are low or high. This analysis may not give the true maximum delay of a circuit because it neglects the possible mismatch between drivers and loads. We propose a new approach for timing analysis in which we first identify the critical path(s) of a circuit using a power-supply-aware timing model. Given these critical paths, we th ...

Keywords: power grid, static timing analysis, voltage fluctuations

33 Timing verification on a 1.2M-device full-custom CMOS design

Jengwei Pan, Larry Biro, Joel Grodstein, Bill Grundmann, Yao-Tsung Yen

June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

Full text available: pdf(333.48 KB) Additional Information: full citation, references, index terms

34 Development of ASIC Chip-Set for High-End Network Processing Application-A Case Study

Sanjeev Patel

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(169.08 KB) Publisher Site Additional Information: full citation, abstract

Choosing the right methodology is a significant step towards successful VLSI designs. Traditional methodologies and tools are no longer adequate to handle large and complex designs. This paper presents a novel design methodology for complex deep-submicron designs, using a case study of the development of a high-end network processing ASIC chip-set. The paper focuses on the synergetic use of the "dual design verification approach", along with static verification methods in achieving defect free s ...

35 Session 8A: static timing analysis: Transistor-level timing analysis using embedded simulation

Pawan Kulshreshtha, Robert Palermo, Mohammad Mortazavi, Cyrus Bamji, Hakan Yalcin

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(86.18 KB) Additional Information: full citation, abstract, references

A high accuracy system for transistor-level static timing analysis is presented. Accurate static timing verification requires that individual gate and interconnect delays be accurately calculated. At the sub-micron level, calculating gate and interconnect delays using delay models can result in reduced accuracy. Instead, the proposed method calculates delays through numerical integration using an embedded circuit simulator. It takes into account short circuit current and carefully chooses the se ...

36 Provably correct high-level timing analysis without path sensitization

Subhrajit Bhattacharya, Sujit Dey, Franc Brglez

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(820.65 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper addresses the problem of true delay estimation during high level design. The existing delay estimation techniques either estimate the topological delay of the circuit

which may be pessimistic, or use gate-level timing analysis for calculating the true delay, which may be prohibitively expensive.We show that the paths in the implementation of a behavioral specification can be partitioned into two sets, SP and UP. While the paths in SP can affect the delay of the circuit ...

37 Timing analysis and verification: SLOCOP-II: a versatile timing verification system for MOSVLSI

P. Johannes, P. Das, L. Claesen, H. De Man

March 1990 **Proceedings of the conference on European design automation**

Full text available: pdf(419.26 KB) Additional Information: full citation, abstract, references

The new SLOCOP-II timing verification system for the accurate performance analysis of MOSVLSI circuits is being presented. The algorithms in SLOCOP-II solve the serious problem of "false paths" that occur in all existing timing verifiers, by taking into account the logic functionallity of the circuits at hand. To allow this for custom MOSVLSI designs, new event determination algorithms based on binary decision tree (BDT) have been developed and are presented in this paper. The algorithms to avoi ...

Keywords: Static timing verification

38 Timing Analysis in Presence of Power Supply and Ground Voltage Variations

Rubil Ahmadi, Farid N. Najm

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(368.16 KB) Additional Information: full citation, abstract, index terms

Given the sensitivity of circuit delay to supply and ground voltagevalues, static timing analysis (STA) must take into account supplyvoltage variations. Existing STA techniques allow one to verifythe timing at different process corners which effectively only considers cases where all the supplies are low or all are high. Cases of mismatch between the supplies of driver and load are not considered. In practice, supply voltages are neither totally independentnor totally dependent. In this work, we ...

39 IEEE 1394a_2000 Physical Layer ASIC

Ranjit Yashwante, Bhalchandra Jahagirdar

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(169.35 KB) Publisher Site Additional Information: full citation, abstract

CN4011A is IEEE 1394a_2000 standard Compliant Physical Layer ASIC. It is a 0.18um mixed-signal ASIC incorporating three analog ports, PLL, reference generator for analog along with the digital control logic. Whole ASIC from specification to GDSII including analog was designed at Controlnet (I) Pvt. Ltd CN4011A has three 1394a_2000 fully compliant ports that support data transfers at 100/200/400 Mbps. It supports repeating of data over on all ports other then receiving port. It's Interoperable wi ...

40 Compiler-directed data prefetching in multiprocessors with memory hierarchies

Edward H. Gornish, Elana D. Granston, Alexander V. Veidenbaum

June 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 4th international conference on Supercomputing**, Volume 18 Issue 3

Full text available: pdf(1.53 MB) Additional Information: full citation, abstract, references, citings, index terms

Memory hierarchies are used by multiprocessor systems to reduce large memory access

times. It is necessary to automatically manage such a hierarchy, to obtain effective memory utilization. In this paper, we discuss the various issues involved in obtaining an optimal memory management strategy for a memory hierarchy. We present an algorithm for finding the earliest point in a program that a block of data can be prefetched. This determination is based on the control and data dependencies in t ...

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41 Circuit effects in static timing: Osculating Thevenin model for predicting delay and slew of capacitively characterized cells
Bernard N. Sheehan
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(76.62 KB) Additional Information: full citation, abstract, references, index terms

To extrapolate from one point to another using a line, one had better get the slope right. In this paper we apply a similar concept to the important problem in Static Timing Analysis (STA) of predicting cell timing for RC loads using capacitive characterization data. Instead of a line we have a Thevenin circuit, and instead of matching slopes we match load sensitivities. We present a table driven, highly accurate cell delay and slew prediction procedure that can improve STA when interconnect eff ...

Keywords: effective capacitance, static timing analysis

42 A design flow for partially reconfigurable hardware
Ian Robertson, James Irvine
May 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 2
Full text available: pdf(698.30 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a top-down designer-driven design flow for creating hardware that exploits partial run-time reconfiguration. Computer-aided design (CAD) tools are presented, which complement conventional FPGA design environments to enable the specification, simulation (both functional and timing), synthesis, automatic placement and routing, partial configuration generation and control of partially reconfigurable designs. Collectively these tools constitute the dynamic circuit switching CAD f ...

Keywords: FPGA, Viterbi decoder, configuration control, dynamically reconfigurable logic (DRL), power estimation, run-time reconfiguration (RTR)

43 Efficient Generation of Delay Change Curves for Noise-Aware Static Timing Analysis
Kanak Agarwal, Yu Cao, Takashi Sato, Dennis Sylvester, Chenming Hu
January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**
Full text available: pdf(267.28 KB) Additional Information: full citation, abstract

Publisher Site

In this paper, we explore the concept of using analytical models to efficiently generate delay change curves (DCCs) that can then be used to characterize the impact of noise on any victim/aggressor configuration. Such an approach captures important noise considerations such as the possibility of delay change even when the switching windows of neighboring gates do not overlap. The technique is model-independent, which we demonstrate by using several crosstalk noise models to obtain results. Furth ...

44 Issues in crosstalk: Clock schedule verification with crosstalk
Hai Zhou
December 2002 **Proceedings of the 8th ACM/IEEE international workshop on Timing issues in the specification and synthesis of digital systems**
Full text available: pdf(157.54 KB) Additional Information: full citation, abstract, references, index terms

Delay variation due to crosstalk has made timing analysis a hard problem. In sequential circuits with transparent latches, crosstalk makes the clock schedule verification even harder. In this paper, we point out a false negative problem in current clock schedule verification techniques and propose a new approach based on switching windows. In this approach, coupling delay calculations are naturally combined with latch iterations. A novel algorithm is given for clock schedule verification in the ...

Keywords: clock schedule, coupling, delay, verification

45 Global harmony: coupled noise analysis for full-chip RC interconnect networks
K. L. Shepard, V. Narayanan, P. C. Elmendorf, Gutuan Zheng
November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(238.78 KB) Additional Information: full citation, abstract, references, citings, index terms
Publisher Site

Noise is becoming one of the most important metrics in the design of VLSI systems, certainly of comparable importance to area, timing, and power. In this paper, we describe Global Harmony, a methodology for the analysis of coupling noise in the global interconnect of large VLSI chips, being developed for the design of high-performance microprocessors. The architecture of Global Harmony involves a careful combination of static noise analysis, static timing analysis, and reduced-order modelling te ...

Keywords: noise, static timing analysis, interconnect

46 A spacing algorithm for performance enhancement and cross-talk reduction
Kamal Chaudhary, Akira Onozawa, Ernest S. Kuh
November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(621.94 KB) Additional Information: full citation, references, citings

47 A crosstalk-aware timing-driven router for FPGAs
Steven J. E. Wilton
February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**
Full text available: pdf(220.27 KB) Additional Information: full citation, abstract, references, citings, index terms

As integrated circuits are migrated to more advanced technologies, it has become clear that crosstalk is an important physical phenomenon that must be taken into account. Crosstalk has primarily been a concern for ASICs, multi-chip modules, and custom chips, however, it will soon become a concern in FPGAs. In this paper, we describe the first published crosstalk-aware router that targets FPGAs. We show that, in a representative FPGA architecture implemented in a 0.18mm technology, the avera ...

Keywords: crosstalk, field-programmable gate arrays, routing algorithms

48 Interface timing verification drives system design

Ajay J. Daga, Peter R. Suaris

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(144.39 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

System design, i.e. the design of board-level circuits andsystems-on-a-chip, focuses on the integration of off-the-shelf andapplication-specific VLSI components. A key aspect of systemdesign is to ensure the satisfaction of component interface timingrequirements. This is necessary for the correct exchange ofinformation among components on a system. We present amethodology for the interface timing verification and subsequenttiming-driven floorplanning of systems. We present results on theapplicat ...

49 A new concept for accurate modeling of VLSI interconnections and its application for timing simulation

B. Wunder, G. Lehmann, K. Müller-Glaser

September 1996 **Proceedings of the conference on European design automation**

Full text available: pdf(415.21 KB) Additional Information: full citation, references, index terms

50 Coping with variability: the end of deterministic design: Death, taxes and failing chips

Chandu Visweswariah

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(145.71 KB) Additional Information: full citation, abstract, references, citings, index terms

In the way they cope with variability, present-day methodologies are onerous, pessimistic and risky, all at the same time! Dealing with variability is an increasingly important aspect of high-performance digital integrated circuit design, and indispensable for first-time-right hardware and cutting-edge performance. This invited paper discusses the methodology, analysis, synthesis and modeling aspects of this problem. These aspects of the problem are compared and contrasted in the ASIC and custom ...

Keywords: Statistical timing, design methodology, parametric yield prediction

51 Power and timing modeling for ASIC designs

W. Roethig, A. M. Zarkesh, M. Andrews

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(44.70 KB) Publisher Site Additional Information: full citation, references, index terms

52 Synthesis, Verification and Test: Timing verification of dynamically reconfigurable logic for the xilinx virtex FPGA series
Ian Robertson, James Irvine, Patrick Lysaght, David Robinson
February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**
Full text available: pdf(610.49 KB) Additional Information: full citation, abstract, references, citings

This paper reports on a method for extending existing VHDL design and verification software available for the Xilinx Virtex series of FPGAs. It allows the designer to apply standard hardware design and verification tools to the design of dynamically reconfigurable logic (DRL). The technique involves the conversion of a dynamic design into multiple static designs, suitable for input to standard synthesis and APR tools. For timing and functional verification after APR, the sections of the design c ...

Keywords: FPGA, dynamic reconfiguration, run-time reconfiguration, verification

53 Power reduction and power-delay trade-offs using logic transformations
Qi Wang, Sarma B. K. Vrudhula, Gary Yeap, Shantanu Ganguly
January 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 1
Full text available: pdf(254.50 KB) Additional Information: full citation, abstract, references, citings, index terms, review

We present an efficient technique to reduce the switching activity in a technology-mapped CMOS combinational circuit based on local logic transformations. The transformations consist of adding redundant connections or gates so as to reduce switching activity. We describe simple and efficient procedures, based on logic implication, for identifying the sources and targets of the redundant connections. Additionally, we give procedures that permit the designer to trade-off power and delay after ...

Keywords: CMOS logic, logic optimization, logic synthesis, low power, power estimation

54 An adaptive timing-driven layout for high speed VLSI
Suphachai Sutanthavibul, Eugene Shragowitz
January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**
Full text available: pdf(863.01 KB) Additional Information: full citation, abstract, references, citings, index terms

An adaptive timing-driven layout system, called JUNE, has been developed. The constructive algorithm, which combines placement with the global routing, constructs a placement satisfying timing and routability constraints. The placement problem for each macro is solved hierarchically as a sequence of two optimization problems followed by an adaptive correction procedure. Experimental results for industrial sea-of-gates chips confirmed effectiveness of this approach.

55 Timing-oriented placement: Multilevel global placement with retiming
Jason Cong, Xin Yuan
June 2003 **Proceedings of the 40th conference on Design automation**
Full text available: pdf(186.09 KB) Additional Information: full citation, abstract, references, citings, index terms

Multiple clock cycles are needed to cross the global interconnects for multi-gigahertz designs in nanometer technologies. For synchronous designs, this requires retiming and pipelining on global interconnects. In this paper, we present a practical solution for simultaneous

retiming and multilevel global placement for performance optimization, based on the theory and algorithms of *sequential timing analysis* (Seq-TA). We extend the Seq-TA to handle gates/clusters with multiple outputs and i ...

Keywords: deep sub-micron, physical hierarchy, placement, retiming

56 Macro-driven circuit design methodology for high-performance datapaths
Mahadevamurty Nemani, Vivek Tiwari
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(90.13 KB) Additional Information: full citation, abstract, references, index terms

Datapath design is one of the most critical elements in the design of a high performance microprocessor. However datapath design is typically does manually, and is often custom style. This adversely impacts the overall productivity of the design team, as well as the quality of the design. In spite of this, very little automation has been available to the designers of high performance datapaths. In this paper we present a new "macro-driven" approach to the design of datapath circ ...

57 Library Compatible Ceff for Gate-Level Timing
B. Sheehan
March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(116.92 KB) Publisher Site Additional Information: full citation, abstract

Accurate gate-level static timing analysis in the presenceof RC loads has become an important problem formodern deep-submicron designs. Non-capacitive loadsare usually analyzed using the concept of an effectivecapacitance, Ceff. Most published algorithms for Ceff,however, require special cell characterization orsupplemental information that is not part of standardtiming libraries. In this paper we present a novel Ceffalgorithm that is strictly compatible with existing timinglibraries. It is also ...

58 Is redundancy necessary to reduce delay
Kurt Keutzer, Sharad Malik, Alexander Saldanha
January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**

Full text available: pdf(1.20 MB) Additional Information: full citation, abstract, references, citings, index terms

Logic optimization procedures principally attempt to optimize three criteria: performance, area and testability. The relationship between area optimization and testability has recently been explored. As to the relationship between performance and testability, experience has shown that performance optimizations can, and do in practice, introduce single stuck-at-fault redundancies into designs. Are these redundancies necessary to increase performance or are they only an unnecessary byproduct ...

59 Power supply, voltage, and frequency management: Dynamic voltage and frequency scaling based on workload decomposition
Kihwan Choi, Ramakrishna Soma, Massoud Pedram
August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

Full text available: pdf(416.31 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a technique called "workload decomposition" in which the CPU workload is decomposed in two parts: on-chip and off-chip. The on-chip workload signifies the CPU clock cycles that are required to execute instructions in the CPU whereas the off-chip workload captures the number of external memory access clock cycles that are required to

perform external memory transactions. When combined with a dynamic voltage and frequency scaling (DVFS) technique to minimize the energy consumpt ...

Keywords: dynamic voltage and frequency scaling, workload decomposition

60 Low Power Design: Enhanced clustered voltage scaling for low power

Monica Donno, Luca Macchiarulo, Alberto Macii, Enrico Macii, Massimo Poncino
April 2002 **Proceedings of the 12th ACM Great Lakes symposium on VLSI**

Full text available: pdf(167.09 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a voltage scaling approach that is based on an enhanced variant of *clustered* voltage scaling originally proposed by Usami and Horowitz ([1]) The results show that subtituting the original depth first strategy with a breadth first one results in improved speed and quality of results. Data are validated through power and timing analysis performed with a commercial tool.

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[PDF] Complexity of minimum-delay gate resizing - VLSI Design, 2001. ...
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phase Figure 1: Variable **circuit**-assembly for variable zi ...
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IEEE STD	IEEE Standard

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